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PCT Application
PCT/JP2002/010177

Translation

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 310201106971	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/JP02/10177	International filing date (*day/month/year*) 30 September 2002 (30.09.02)	Priority date (*day/month/year*)
International Patent Classification (IPC) or national classification and IPC H01L 21/60		
Applicant HITACHI, LTD		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand 30 September 2002 (30.09.02)	Date of completion of this report 09 July 2003 (09.07.2003)
Name and mailing address of the IPEA/JP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP02/10177

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed

☒ the description:

pages 1-13, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

☒ the claims:

pages 2-9, 12-16, as originally filed

pages _____, as amended (together with any statement under Article 19

pages _____, filed with the demand

pages 1, 10, 11, 17-20, filed with the letter of 30 June 2003 (30.06.2003)

☒ the drawings:

pages 1-22, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

☐ the sequence listing part of the description:

pages _____, as originally filed

pages _____, filed with the demand

pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRE[redacted]NARY EXAMINATION REPORT

Inter[redacted]al application No.
PCT/JP 02/10177

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims		NO
Inventive step (IS)	Claims		YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims		NO

2. Citations and explanations

Document 1: JP 2002-208668 A (Hitachi, Ltd.), 26 July 2002, paragraphs 0043, 0045, 0053 and 0149, and fig. 1-3

Document 2: JP 2000-21920 A (Sony Corp.), 21 January 2001, paragraph 0023 and Fig. 3 and 4

Document 3: JP 2001-313459 A (TDK Corp.), 09 November 2001, paragraphs 0074 and 0075, and fig. 9

The inventions that are set forth in claims 1-5, 7-15 and 17-20 do not involve an inventive step in the light of documents 1 and 2 cited in the international search report. Document 1 does not make any specifications pertaining to the height or the horizontal length of the bonding wire; however, with consideration of miniaturizing and thinning down the device, it would be easy for a person skilled in the art to configure the inventions that are set forth in claims 1-5, 7-15 and 17-20 by configuring the semiconductor device that is disclosed in document 1 using a loop height and a wire length such as those suggested in document 2. In addition, the range for the coefficient of elasticity that is set forth in claim 8 is not specifically disclosed in document 1, but does fall within the range that is suggested therein. Therefore, it would be easy for a person skilled in the art to select

such a range.

Furthermore, documents 1 and 2 do not disclose the technical concept of preventing the wire from becoming disconnected as a result of the thermal contraction of the low-elasticity resin. However, it is possible to configure the inventions that are set forth in claims 1-5, 7-15 and 17-20 in the light of different concepts, such as those indicated above; therefore, the inventions in question cannot be considered to involve an inventive step.

The inventions that are set forth in claims 6 and 16 do not involve an inventive step in the light of documents 1-3 cited in the international search report. It would be easy for a person skilled in the art to configure the Pb-free reactive solder that is disclosed in document 1 from a solder material such as that which is disclosed in document 3.

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claims 1-16 and 19-20 are not fully supported by the description. That is to say, the disclosures of claims 1-16 and 19-20 can be interpreted as including cases wherein substances other than gold wire are used to configure the bonding wire; however, in such cases the technical significance of specifications such as 'a height of 0.2mm or less' in relation to the bonding wire are not fully supported.

What is claimed is:

1.(amended) A semiconductor device comprising:

a semiconductor chip;

a wiring board over which said semiconductor chip connected by solder is mounted;

a plurality of bonding wires for connecting surface electrodes of said semiconductor chip to terminals of said wiring board corresponding thereto; and

a sealing section in which said semiconductor chip and said plurality of bonding wires are covered and sealed with resin, said sealing section being formed of an insulating elastic resin,

wherein said elastic resin has an elastic modulus of 1 to 200 MPa at a temperature of 150°C or higher, and a height of said bonding wire from a main surface of said semiconductor chip to a top of said bonding wire is 0.2 mm or less.

2. The semiconductor device according to Claim 1,

wherein a height of said bonding wire from the main surface of said semiconductor chip to the top of said bonding wire is from 0.1 mm or more to 0.2 mm.

3. The semiconductor device according to Claim 1,

wherein a wire horizontal distance from a bonding start point to an end point of said bonding wire is 1.5 mm or less.

4. The semiconductor device according to Claim 3, wherein said wire horizontal distance is from 0.5 mm to 1.5 mm.

5. The semiconductor device according to Claim 1, wherein said elastic resin is silicone resin.

6. The semiconductor device according to Claim 1, wherein chip components having connection terminals formed on both ends thereof are connected to said wiring board by solder, and said solder is mainly comprised of tin (Sn) and antimony (Sb).

7. The semiconductor device according to Claim 1, wherein chip components having connection terminals formed on both ends thereof are connected to said wiring board by solder, and said solder does not contain lead (Pb).

8. The semiconductor device according to Claim 1, wherein said elastic resin has an elastic modulus of 5 to 10 MPa at a temperature of 150°C or higher.

9. The semiconductor device according to Claim 1, wherein a recess is formed in said wiring board and said semiconductor chip is disposed in said recess.

10.(amended) A semiconductor device comprising:

a semiconductor chip;

a wiring board over which said semiconductor chip connected by solder is mounted;

a plurality of bonding wires for connecting surface electrodes of said semiconductor chip to terminals of said wiring board corresponding thereto; and

a sealing section in which said semiconductor chip and said plurality of bonding wires are covered and sealed with resin, said sealing section being formed of a silicone resin which is an insulating elastic resin with an elastic modulus of 1 to 200 MPa at a temperature of 150°C or higher,

wherein a height of said bonding wire from a main surface of said semiconductor chip to a top of said bonding wire is 0.2 mm or less, and a wire horizontal distance from a bonding start point to an end point of said bonding wire is 1.5 mm or less.

11.(amended) A semiconductor device comprising:

a semiconductor chip;

a wiring board over which said semiconductor chip connected by solder is mounted;

a plurality of bonding wires for connecting surface electrodes of said semiconductor chip to terminals of said wiring board corresponding thereto; and

a sealing section in which said semiconductor chip and said

plurality of bonding wires are covered and sealed with resin, said sealing section being formed of an insulating elastic resin,

wherein said elastic resin has an elastic modulus of 1 to 200 MPa at a temperature of 150°C or higher, and a height of said bonding wire from a bonding start point to a top of said bonding wire is 0.2 mm or less.

12. The semiconductor device according to Claim 11,

wherein a wire horizontal distance from a bonding start point to an end point of said bonding wire is 1.5 mm or less.

13. A semiconductor device comprising:

a semiconductor chip;

a wiring board over which said semiconductor chip is mounted;

a plurality of bonding wires for connecting surface electrodes of said semiconductor chip to terminals of said wiring board corresponding thereto, said bonding wire having a height of 0.2 mm or less from a main surface of said semiconductor chip to a top of said wire; and

a sealing section in which said semiconductor chip and said plurality of bonding wires are covered and sealed with resin, said sealing section being formed of an insulating elastic resin with an elastic modulus of 1 to 200 MPa at a temperature of 150°C or higher,

wherein said semiconductor device is connected to a mounting board by solder.

14. The semiconductor device according to Claim 13, wherein a wire horizontal distance from a bonding start point to an end point of said bonding wire is 1.5 mm or less.

15. The semiconductor device according to Claim 13, wherein said semiconductor device is connected to said mounting board by solder containing no lead (Pb).

16. The semiconductor device according to Claim 13, wherein said semiconductor device is connected to said mounting board by solder which is mainly comprised of tin (Sn), silver (Ag), and copper (Cu).

17.(added) The semiconductor device according to Claim 1, wherein said bonding wires are made of gold.

18.(added) The semiconductor device according to Claim 10, wherein said bonding wires are made of gold.

19.(added) The semiconductor device according to Claim 10, wherein the chip components are connected onto said wiring board by solder.

20.(added) The semiconductor device according to Claim 11, wherein the chip components are connected onto said wiring board by solder.